

● PRINTER RUSH ●

(PTO ASSISTANCE)

Application : <u>09960572</u>	Examiner : <u>Tran</u>	GAU : <u>2614</u>
From: <u>MPB</u>	Location: <u>(IDC) FMF FDC</u>	Date: <u>09/06/05</u>
Tracking #: <u>epm 09960572</u>		Week Date: <u>06/20/05</u>

DOC CODE	DOC DATE	MISCELLANEOUS
<input type="checkbox"/> 1449	_____	<input type="checkbox"/> Continuing Data
<input type="checkbox"/> IDS	_____	<input type="checkbox"/> Foreign Priority
<input type="checkbox"/> CLM	_____	<input type="checkbox"/> Document Legibility
<input type="checkbox"/> IIFW	_____	<input type="checkbox"/> Fees
<input type="checkbox"/> SRFW	_____	<input type="checkbox"/> Other
<input type="checkbox"/> DRW	_____	
<input type="checkbox"/> OATH	_____	
<input type="checkbox"/> 312	_____	
<input checked="" type="checkbox"/> SPEC	<u>09/21/01</u>	

[RUSH] MESSAGE:

please provide missing serial numbers on the following pages:

a) page 1, lines 5 and 6 ; and

b) page 5, line 19.

Thank you

[XRUSH] RESPONSE:

A. - Done

B. - Done

INITIALS [Signature]

NOTE: This form will be included as part of the official USPTO record, with the Response document coded as XRUSH.

REV 10/04

BLOCK MOVE ENGINE WITH GAMMA AND COLOR CONVERSIONS

Cross Reference to Related Applications

5 The present application may relate to co-pending
application Serial No. 09/960,578 filed concurrently (Attorney
Docket 1496.00119) and Serial No. 09/960,771 filed concurrently
(Attorney Docket 1496.00154), which are each hereby incorporated by
reference in their entirety.

Field of the Invention

10 The present invention relates to a method and/or
architecture for implementing block modify and move engines (BMMEs)
generally and, more particularly, a method and/or architecture for
implementing color and gamma correctors that may be used within the
15 data modification section of a BMME.

Background of the Invention

20 The implementation of a block move engine (BME) (a bit
blitter or blitting engine) for rapidly copying blocks of graphics
data from one location in memory to another is generally used for

component. The correction circuit 104 may also receive the coefficient signals COEFFS, the offset signals OFFSETS and the signal GAMEN. The delay circuit 102 may present a portion of the signal FRONTOUT and the correction circuit 104 may present another portion of the signal FRONTOUT. The various signals of the present invention may be implemented as single-bit or multi-bit signals.

Color correction and gamma correction may both be valid operations on color components of graphics and video data. However, such correction may not be relevant to alpha data. A bypass path via the delay 102 may be provided for the alpha data ALPHA, when applicable. Delay for color components CC through the correction circuitry 104 may be matched by the delay 102 for the alpha channel ALPHA. The color components CC may be RGB or YUV for most graphics and video operations. However, other appropriate color components may be implemented to meet the design criteria of a particular implementation.

Referring to FIG. 2, a context of the present invention is shown. The details of FIG. 2 are described in co-pending application Serial No. 09/960,771 filed concurrently (Attorney Docket 1496.00154).